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8. A memory controller according to claim 1,  
wherein the data bit width of said memory section is  
made equal to  $2n$  times of the bit width of said input  
data and data for a number of frames up to as many as  
5 (2n-2) times of the number of input pixels can be read  
out of said memory section for said input data while  
the frequency of accessing said memory section can be  
reduced to a half or less than a half of the video  
signal input frequency.

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9. A memory controller according to claim 3,  
wherein the bit width of said input data is equal to 8  
bits and said  $n$  is equal to 3, whereas said data bit  
width of said memory section is equal to 24.

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10. A memory controller according to claim 3,  
wherein the bit width of said input data is equal to 8  
bits and said  $n$  is equal to 4, whereas said data bit  
width of said memory section is equal to 32.

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11. A memory controller according to claim 1,  
wherein said memory section comprises a plurality of  
memory units.

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12. A liquid crystal display apparatus  
comprising:

an interface for transforming various video

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signals and transmission signals standard video signals;

a decoder for transforming standard video signals into video signals for displaying images on liquid crystal;

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a liquid crystal display panel; and

a drive section for driving said display panel according to said video signals, characterized in that

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said decoder includes a memory controller comprising a serial/parallel converter section for converting serial input data into parallel data, an FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the data read out from the frame memory section.

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ADD  
B<sub>1</sub>

ADD  
D<sub>1</sub>